Abstract

Method for synchronizing a plurality of digital input signals

The invention relates to a method for synchronizing a plurality of digital input signals which are formed by sampling with the aid of a dedicated operating clock in each case.

In order to be able to carry out such a method reliably with a relatively low outlay, according to the invention digital auxiliary signals (xd(nk+j), (yd(nk+j)) are formed by sampling the digital input signals (x(k)) with the aid of a common postprocessing clock, use being made of a postprocessing clock which is at least twice as fast as the fastest operating clock; synchronized digital output signals (x(m), y(m)) which correspond to the digital input signals (x(k)) are formed by means of interpolating each digital auxiliary signal (xd(nk+j), yd(nk+j)).

Figure 1